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Multiplication Techniques used in Vedic Mathematics

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Abstract:

Indian mathematics has an ancient technologies that is 'Vedic mathematics' which as a unique technique of calculations based on simple rules and principles which have 16 Formulae (Sutras). This paper concern on A high speed complex multiplier design (ASIC) that is using Vedic Mathematics. From ancient Indian mathematics "Vedas", adopted the idea for designing multiplier and adder subtractor unit. In which, multiplication is an important factor in arithmetic operation and is carried out in number of Digital Signal Processing applications. For execution, multiplier take a long time, so need of fast multiplier to save execution time. In this paper, discuss about the multiplication using Ancient Indian Vedic Mathematics multiplication techniques. In techniques, describes the Nikhilam Sutra, Urdhva Tiryakbhyam and Karatsuba-ofman and technique is obtained from performance analysis due to which solving a whole range mathematical problems by its high speed. It also discuss about the convolution that is a formal mathematical operation, just as addition, multiplication and integration.

Keywords: *Complex Multiplier, Vedic Mathematics, Convolution, A high speed complex multiplier design (ASIC)*

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Introduction

In arithmetic operations, Complex Multiplication is an important fundamental and immense function in Digital Signal Processing (DSP) and Image Processing (IP). Complex number multiplication is performed using four real number multiplications and two additions/subtractions. It carry needs to be propagate from least significant bit (LSB) to most significant bit (MSB) in real number processing in case of binary partial products added. After binary multiplications, addition and subtraction limit the overall speed. Multiply and Accumulate (MAC) is Multiplication-based operations and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions (CIAF) currently executed in many Digital Signal Processing (DSP) that have applications such as Fast Fourier Transform (FFT), convolution, filtering and in microprocessors in its arithmetic and logic unit. Multiplication dominates the execution time of most DSP algorithms, so its need of high speed multiplier. In determining the instruction cycle time of DSP chip, multiplication time is still dominant factor.

As a result of expanding computer and signal processing applications, demand has been increase for high speed processing. In many real-time signal and image processing applications, higher throughput arithmetic operations are important to achieve desired performance. Multiplication is one of the major key of arithmetic operations and development of fast multiplier circuit has been a subject of interest over decades. Multiplier is based on Vedic Mathematics is one of the fast and low power multiplier. It is a building blocks of processor design and generally called as heart of DSP. Modern multipliers speed of computation decrease as an input increase. Today, many multipliers are available such as array multiplier, combinational multiplier, serial and parallel multiplier and many more. By using Vedic math, building high speed multipliers for processor design is done. Filtering is generally used in DSPs and is applied in many applications such as speech processing etc. In DSP, digital multiplier are most commonly used components such as fast, reliable and efficient that are utilized to implement any operation.

A multiplier of size n bits has n2 gates. In DSP applications, performed multiplication algorithms that have two major concern which is latency and throughout from delay perspective. Latency is real delay of computing function, a measure of how long the inputs to a device are stable is the final result available on outputs. But in given period of time, throughput is the measure of how many multiplications can be performed, multiplier is not only a high delay block but it also a major source of power dissipation.

History of Vedic Mathematics

Indian system of mathematics are exist in Ancient Indian sculptures (Vedas) which was rediscovered in early 20th century. It includes Vedic mathematical formulae which can be applied to various branches of mathematics. By using Vedic sutras, conventional mathematical algorithms are simplified and also optimized. It covers several modern mathematical terms including trigonometry, arithmetic, quadratic equations, geometry (plane, co-ordinate), factorization and even calculus. Now a day, increasing the demand of digital signal processing, image processing and other heavy computational applications require faster computation by processor. Division and multiplication are one of the arithmetic operations which require heavy calculations. Traditional methods require a lot of time to solving problem in which include array, carry save, Wallace tree booth etc. Multiplier architecture based on all these methods that are not efficient in term of area, speed, power. Vedic mathematics contain some steps to solve multiplication rather than the traditional multiplication. Vedic mathematics is frequently based on 16 sutra which dealing with various branches of mathematics such as algebra, geometry, arithmetic etc.

Vedic Mathematics

By ancient sages of India, discovered Vedic mathematics that is an ancient Indian mathematics. In 1965, it was rediscovered by Jagadguru shankaracharya Bharathi Krishna Teerthji maharaja (1884-1960). Mental calculation of Vedic mathematics is called by Swaiji. Vedic mathematics consist of 16 sutras (formulae) and 16 sub-sutras (sub-formulae) and these sutras cannot be finding in Atharva Veda. From Atharva Veda, these sutras were derived by ancient sages of India. Vedic mathematics is a unique system of computation that is based on simple rules and principles due to which solving the complication mathematical calculation in few seconds. This filed seems to be very interesting and give computation algorithm by which we can solve difficult mathematical equations of various branches in engineering such as computing.

The term ‘Vedic’ has been taken from Sanskrit word ‘Veda’ that have meaning a bunch of knowledge or collection of all knowledge. It is a logical tool and deals with several simple as well as complex mathematical operations. The advantages of Vedic method is given below:

- Reduces the complexity of solving equation
- Within 5 seconds, person to solve complex equation
- Finger counting and scratches are avoided
- 10-15 times faster, solving higher level equations

Vedic mathematics consist of 16 sutras and 13 sub-sutras and these are used to solve equations which is given in below:

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
3. Ekadhikina Purvena – By one more than the previous one.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
6. Chalana-Kalanabyham – Differences and Similarities.
7. Parvarya yojayet – Transpose and adjust.
8. Puranapuranabhyam – By the completion or no completion.
9. Sankalana- vyavakalanabhyam – By addition and by subtraction.
10. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
11. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
12. Urdhava-tiryagbhyam – Vertically and crosswise.
13. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
14. Vyashtisamanstih – Part and Whole.
15. Yaavadunam – Whatever the extent of its deficiency
16. Shesanyankena Charamena – The remainders by the last digit.

13 Sub-Sutras are:

1. Shishyate Sheshsamjnah
2. Anurupyena
3. Adyamadye Nantyamantyena
4. Vestanam
5. Lopanasthapanabhyam
6. Yavadunam Tavadunam
7. Antyatoreva
8. Yavadunam Tavadunikutya Vargankach Yojayet
9. Kevalaih Saptakam Gunyat
10. Antyayordhshakepi
11. Samucchayagunitah
12. Gunitasamucchyah Samucchayagunitah.
13. Vilokanam

Vedic multiplier is based on Vedic multiplication formulae (Sutras) and these sutras are used for multiplication of two numbers in decimal number system. These same formulae applied on the binary number system. In this paper concentrating on “"Urdhva-tiryakbyham", "Nikhilam Navatascaramam Dasatah" and “Karatsuba-Ofman”. Vedic multiplication based on some algorithms, some are discussed below:

Urdhva Tiryakbhyam sutra

Ancient Indian Vedic Mathematics contain some sutras in which Urdhva Tiryakbhyam sutra is contain in which multiplier is based on it. This sutra is normally multiplication formula that is applicable to all cases of multiplication. This sutras have literally means “Vertically and crosswise” and based on a novel concept through which generation of all partial products can be done with simultaneous addition of these partial products. This algorithm can be generalized for n*n bit number. In parallel, the partial products and their sums are calculated, the multiplier is independent of clock frequency of processor. To calculate the product, multiplier will require same amount of time and hence is independent of clock frequency. It has advantage that it reduce the need of microprocessor to operate at increasingly high clock frequencies but a higher clock frequency normally result in increased processing power and its disadvantage is that it also increases power.

Nikhilam Sutra

Nikhilam Sutra factually means “all from 9 and last from 10”. It is applicable to all cases of multiplication and when numbers are involved in large, it is more

efficient. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, lesser the complexity of the multiplication, larger is the original number. Here, we illustrate this sutra by multiplication of two decimal numbers (96 * 93) where the chosen base is 100 which is nearest to and greater than both these two numbers.

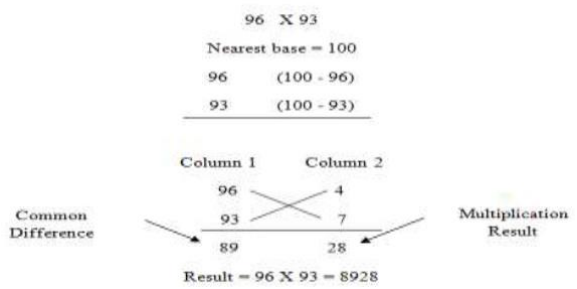

Figure: Multiplication using Nikhilam Sutra

Karatsuba-Ofman

This type of sutra is considered as one of the fastest ways of multiplication of long integers and based on divide and conquers strategy. A multiplication of 2n digit integer is reduced to two n digit multiplications, one n digit subtractions, two (n+1) digit multiplication, two left shift operations, two n digit additions and two 2n digit additions.

Complex Multiplier

By using parallel adders and subtractors, complex multiplier has been designed by Saha. Complex multiplier design by direct method of implementation and it is done using Vedic Multipliers and Vedic subtractors. Multiplication Algorithm

<Input>

A and B: Multiplicand and multiplier respectively. Both are complex numbers .A=Ar+ jA; and B =Br +jB; (here all are N Bit unsigned numbers).

Step l. Select the appropriate base using RSU.

Step2. Multiply the numbers and then add or subtract them to obtain the real and the imaginary part of the result.

<Output>

Result: Cr and C; are the real and imaginary part of complex number.

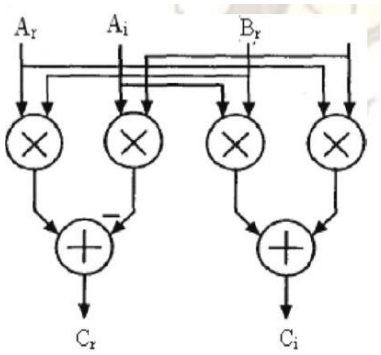

Figure: Implementation of Complex multiplier design

Convolution

It is a mathematical way of combining two signals to form a third signal. It is used of 4 bit Vedic Multiplier in which 4*4 multiplier is made by using 4, 2*2 multiplier blocks. Here, the multiplicands using the bit size that n=4 which come result is of 8 bit size. The input is broken into smaller chunks of size of n/2 = 2, for both inputs that is a and b. These newly formed lumps of 2 bits are given as input to 2*2 multiplier block and result produced 4 bits, which are output produced from 2x2 multiplier block are sent for addition to an addition tree.

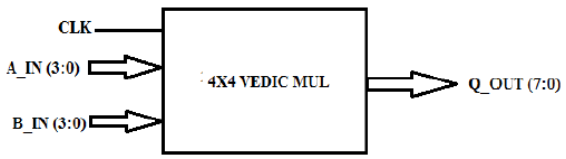

Figure: 4 bit Vedic Multiplier

Little modification is required for higher number of bits in input and in input, divide the number of bit in equal in two parts. A novel multiplier architecture based on Urdhva Triyagbhyam Sutra of Ancient Indian Vedic Mathematics is fixed into proposed method of convolution to improve its efficiency in terms of speed and area.

Deconvolution

Deconvolution is an operation that takes two functions one input is convolved sequence y(n) and other input one is h(n), and produces a single function output x(n). For Deconvolution a direct method is presented for performing Deconvolution of two finite length sequences. The basic recursive Deconvoltion method is used for finding Deconvoltion of finite length sequences.

Review of Literature

Ismail and Sivasubramniam 2010, dictated that Vedic mathematics has positive effects on pupils by solving the multiplication problem in less time. Pupil must be reminded that the Vedic method will fail if applied on which they are out of work product of two numbers less than or equal to five. Vedic method would be used in mechanical manner as one uses a tool such as a calculator.

Somani et.al 2012, concluded that Vedic Multiplier consist 16 Sutras in which one Urdhva Tiryagbhyam, is smallest, fastest multiplier using low power. This type of sutras is dominated the other type of sutras as number of bits increases in multiplication. The traditional multipliers can be replaced by Urdhva Tiryagbhyam due to various factors such as space, timing efficiency, lesser area and PDP. In Urdhva Tiryagbhyam, consist of power, PDP and Delay which is reduced by 28.84%, 24.65% and 46.38% compare to Hierarchical Array (HAM) and 10.43%, 17.98% and 26.54% compare to Urdhva Tiryagbhyam multiplier respectively.

Nagaraju, Prakash and Bhaskar 2013, stated that novel complex number multiplier design based on formulae of the ancient Indian Vedic Mathematics that is highly suitable for high speed complex arithmetic circuits which are having wide application in VLSI signal processing. In spice spectre, implementation was done and compared with mostly used architecture like distributed. The developed Complex Multiplier design is modelled and is simulated using Modelsim tool.

Dighorikar and Haridas 2014, concluded that multiplier is very important element in any processor design and a processor spends considerable amount of time in performing and generally the most area consuming. Multiplier contain a major design issue which is optimizing the area and sped. By using new techniques, improvement in multiplication speed which can greatly improve system performance.

Jain 2014, stated that in this paper, focus on the different designs of multipliers that are focused on Vedic Mathematical sutras. Vedic mathematics sutras are used in place of different arithmetic operation such as division and multiplication etc. and it is used in different applications like image processing, digital signal processing and computation of heavy calculations. It is more focus on Vedic mathematics sutras that are used in multiplier will give better result and have a lot of space in computer field.

Dharmannavar and Dharmambal 2015, by using Matlab, implementation of IIR and FIR (Infinite Impulse Response Filter). In Graphical user interface window, FIR filter design that is based on window, is implemented by use of Urdhwa Tiryakbyam multiplication Vedic sutra. By seeing result, come to know that the execution time taken by Vedic method using use of Urdhwa Tiryakbyam multiplication is less compared to conventional method. These Vedic formulae are much more efficient to conventional method. Using filter technique which is use of Urdhwa Tiryakbyam multiplication method to improve the techniques that is used in Image processing, network secutiy, stenography.

Conclusion

Ancient Indian Vedic Mathematics developed novel complex number multiplier which is design based on formulas and it have highly suitable for high speed complex arithmetic circuit. In this paper, discuss about the techniques on multiplication factors (16 sutras) due to which mathematics equations are solved in less time and this techniques are very suitable tool. Students are satisfied from these techniques and they says that these technique are very helpful for them. With the help of Vedic Mathematics, calculating the linear convolution and Deconvolution that are easy to perform and learn.

References:

Basker, P. “High Speed Design of Complex Multiplier Using Vedic Mathematics.” *International Journal of Innovative Research in Technology, Science & Engineering (IJIRTSE),* vol. 1, no. 5, July 2015, pp. 38–44.

Dharmannavar, Kavita H., and Dharmambal. “The Application of Vedic Mathematics For High Speed Multiplier In Fir Filter Design.” *International Journal of Engineering Research and General Science,* vol. 3, no. 3, 2015, pp. 364–371.

Dighorikar, Karishma P., and S. L. Haridas. “Area Efficient Architecture for Convolution Using Vedic Mathematics.” *International Journal of Science and Research (IJSR),* vol. 3, no. 3, Mar. 2014, pp. 28–30.

Hussain, S. Nazeer, and G. Sudhakiran. “Vedic Mathematics Applications in DSP: Convolution and De-Convolution.” *International Journal of Advanced Research in Computer Science and Software Engineering,* vol. 6, no. 4, Apr. 2016, pp. 358–363.

Jain, Shivangi, and V. S. Jagtap. “Vedic Mathematics in Computer: A Survey.” *International Journal of Computer Science and Information Technologies,* vol. 5, no. 6, 2014, pp. 7458–7459.

Kavita, and Umesh Goyal. “Performance Analysis of Various Vedic Techniques for Multiplication.” *International Journal of Engineering Trends and Technology*, vol. 3, no. 4, 2013, pp. 231–235.

Kumar, G. Ganesh, and V. Charishma. “Design of High Speed Vedic Multiplier Using Vedic Mathematics Techniques.” *International Journal of Scientific Research and Publications*, vol. 2, no. 3, Mar. 2012, pp. 1–5.

Nagaraju, M., et al. “High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics.” *International Journal of Engineering Research and Applications (IJERA),* vol. 3, no. 1, 2013, pp. 1079–1084.

Shri, P. Padma, et al. “VLSI Design of High Performance Complex Multiplier.” *International Refereed Journal of Engineering and Science (IRJES),* vol. 1, no. 4, Dec. 2014, pp. 68–75.

Somani, Arushi, et al. “Compare Vedic Multipliers with ConventionalHierarchical Array of Array Multiplier .” *International Journal of Computer Technology and Electronics Engineering (IJCTEE),* vol. 2, no. 6, Dec. 2012, pp. 52–55.

Syed, Syed Azman bin, and Pumadevi Sivasubramniam. “Multiplication with the Vedic Method .” *International Conference on Mathematics Education Research* , 2010, pp. 129–133.